AMENDMENTS TO THE CLAIMS

1. (currently amended) A memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;

a composite gate insulator layer overlying the substrate;

a metal floating gate overlying the ~~substrate~~ gate insulator, wherein an upper portion of the metal floating gate is oxidized, thereby defining a metal oxide inter-gate insulator layer; and

~~a metal oxide inter-gate insulator layer formed over the metal floating gate; the inter-gate insulator layer having a dielectric constant that is greater than a dielectric constant of silicon dioxide; and~~

a control gate formed on top of the inter-gate insulator layer.

2. (canceled)

3. (currently amended) The transistor of claim 1 ~~2~~ wherein the composite gate insulator layer is comprised of deposited aluminum oxide – aluminum – aluminum oxide wherein the upper aluminum oxide layer is the oxidized upper portion of the metal floating gate ~~grown by oxidation~~.

4. (original) The transistor of claim 3 wherein the aluminum oxide is grown by low temperature oxidation.

5. (currently amended) The transistor of claim 1 ~~2~~ wherein the composite gate insulator layer is comprised of deposited aluminum oxide – aluminum – deposited aluminum oxide.

6. (currently amended) The transistor of claim 1 ~~2~~ wherein the composite gate insulator layer is comprised of PbO – Pb – PbO wherein the upper PbO layer is the oxidized upper portion of the Pb layer ~~is grown by oxidation of Pb~~.

7. (original) The transistor of claim 1 wherein the control gate is comprised of a metal.

8-29. (cancelled)